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Bi-Directional Converter with ZSPL Technology for Flywheel Energy Storage System

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Abstract
A bi-directional converter (BDC) is important in applications where energy storage devices are involved. Such applications include transportation, battery less UPS, Flywheel Energy Storage (FES) systems etc. Bi-directional power flow through buck and boost mode operation along with high power density and proficiency are significant requirements of such systems. This paper presents a new BDC topology using MOSFET with a novel control logic execution to attain zero switching losses through Zero Voltage Transition (ZVT) and Zero Current Transition (ZCT) techniques. The presented scheme assures Zero Switching Power Loss (ZSPL) for both buck and boost modes of operation of the BDC. The scheme is easy and achieves ZSPL during both turn-on and turn-off of the devices ensuing in improved efficiency and reduced EMI problems. The essential principle of operation, analysis, and design process are proposed for both buck and boost modes of operation. A design example is presented.

1. Introduction

A Bi-directional converter is an important part of applications where energy storage devices are used. This paper focuses on one such application where flywheel is used as the energy storage device. A FES system is shown in Fig. 1. The electrical machine is coupled to the flywheel. The electrical machine used in this paper is Brushless DC machine. The BLDC machine coupled to a flywheel is henceforward called as "FES machine' in this paper. This machine extracts the power from dc bus and speed up the flywheel in motoring mode to store the energy; the BDC acts as a voltage buck converter (buck mode). The same machine releases the flywheel in generation mode to return back the energy to the dc bus; the BDC acts as a voltage boost converter (boost mode).

As shown in Fig. 1. Typical FES system and sources of losses Higher power density (compactness) and efficiency are important necessities of such systems [11]. High power densities in switched mode power converters can be accomplished by switching at high frequencies. Higher efficiency can be achieved by taking appropriate measures to reduce the losses. Losses due to switching of devices at higher frequencies contribute significantly to the total loss of the BDC particularly at lower generator speeds (lower Causes and mechanism of switching power loss in a semiconductor device are already well documented. Switching power loss can be reduced either by Zero Voltage Switching (ZCS/ZCT) method or Zero Current Switching (ZCS/ZCT) method depending upon whether the voltage across the device is made zero during the turn ON or the current through the device is made zero during the turn ON or the current through the device is made zero during the turn OFF transition. It may be noted that in ZVS/ZCS, the resonant circuit doesn't come in series with the main switch – rather it comes into depiction only during the transitions (ON TO OFF AND OFF TO ON). This makes ZCT/ZCT topologies suitable for PWM applications. In ZCT technique, the current through the switching device becomes negative (i.e. anti-parallel diode conducts) during the switching transition, making it a "true" Zero Switching Power Loss (ZSPL) as compared to ZVS/ZCS.

In case of FES systems, the bi-directional converter where IGBT or MOSFET is the preferred switching device is required to have ZCT switching in both buck and boost mode of operation to achieve true ZSPL operation. Generally, the configurations used in these BDC configurations include coupled inductors based converters, series resonant circuits and half-bridge circuits with PWM. Investigations into major families of isolated BDCs which employ soft-switching techniques are reported in [6]. One such resonant tank isolated BDC emphasizes ZVS for input side chopper and ZCS for output rectifier-switches is proposed in [7] and another ZVS-PWM non-isolated bi-directional converter dc-dc converter with steep conversion ratio is proposed using auxiliary circuits [8]. In both the proposals, ZVS is achieved in both buck and boost modes of operation but only for turn on transition.

From the literature survey carried out, it is observed that a true ZSPL scheme for a BDC, which makes both turn off and turn on losses exactly zero is not available.

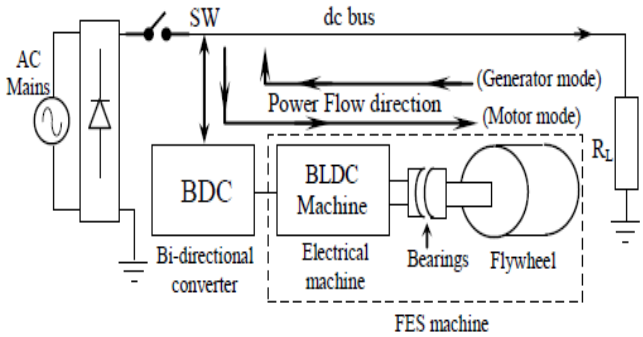

Fig. 1. Typical FES system and sources of losses Higher power density

2. New ZSPL Topology For Bi-Directional Converter

A new ZSPL BDC topology is proposed in this paper that renders improved efficiency. In this topology the devices used are MOSFETs as main devices for carrying load current and also as auxiliary devices. Bidirectional converters which are used in energy storage systems are basically DC-DC converters. A typical BDC consists of two switches. While one switch is used for stepping down the voltage and making the power floe from the dc bus to FES machine, the other switch is used for boosting the voltage making the power flow from FES induced voltage) in an FES system [4].
machine to the dc bus.

2.1. Proposed scheme

The circuit configuration used here is a modified version of the McMurray Bed ford circuit. The new topology uses MOSFET as the main as well as auxiliary device. The current impulse in the resonant circuit has a natural zero crossing. In terms of power loss, a MOSFET has two advantages over an IGBT: purely resistive without an offset voltage in conduction and no tail current at turn-off. Power loss can thus be condensed by replacing the lower IGBT with a MOSFET. Since a MOSFET has no offset voltage in conduction, the conduction loss becomes much less as the load decreases. The design approach, control logic attainment , and selection of values of resonant circuit (LCL) are explained in section IV of this paper. The proposed topology, in conjunction with developed control logic, is able to achieve ZSPL for both buck and boost mode of operation.

2.2. Working principle and operation of the proposed topology

Fig. 2 shows the equivalent circuit of the system depicted in Fig. 1. For the sake of simplicity only one phase of the 3-phase FES machine and BDC is shown. The dc bus is energized from the voltage obtained by rectifying the ac mains voltage. The FES machine is connected to the dc bus through the switches S_1 and S_2 as shown in

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Fig. 2.In motor mode, the switch S along with D_2 is used for bucking the voltage of dc bus to drive the FES machine. Similarly in generator mode, the switch S_2 along with D_1 is used for boosting the voltage output of the FES machine

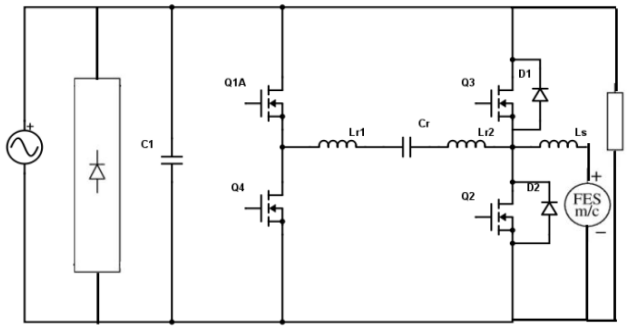


Fig. 2. Equivalent circuit diagram of one phase of the new ZSPL topology Bi-directional converter

Switching assisted by ZCT is realized through the oscillating action of an LCL circuit which is triggered by an auxiliary switch. S_1, S_2 are the main switches and S_{1A}, S_{2A} are the auxiliary switches as shown in Fig. 2. Also, there are anti-parallel diodes D_1 and D_2 for the switches S_1 and S_2 respectively. The trigger control logic for these four switches is implemented in such a way that, the current is made to flow through the diode which is connected anti-parallel to the main device whenever the main device is required to be turned on or turned off. When the voltage across it is zero the main device to go from OFF state to ON state and from ON state to OFF state when the current through it is zero. This results in an ideal ZSPL switching of the device. This topology can be used for energy transfer from dc bus to FES machine (known as buck mode) as well as from FES machine to dc bus (known as boost mode).

3. Analysis and Design of the Proposed Scheme

Comprehensive analysis of turn ON and turn OFF commutation for buck and boost modes of operation of presented topology is carried out in this section.

3.1. Switching waveforms and Analysis in Buck mode

In this mode the power flows from the dc bus to the FES machine. The switch S_1 is gated with high frequency pulses whose width is adjusted to get the required voltage at the input of FES machine. Control pulses and anticipated waveforms across the power components are shown in Fig. 3. By referring to Fig. 3 and 4, analysis of the circuit is carried out as:

Mode 1(t_0-t_1)

The capacitor C_r is charged with the polarity as shown in Fig. 4(a).

Mode 2[$t_1 – t_2$]

The auxiliary switch S_{1A} (MOSFET) is turned on (at instant t_1) before the switch S_1 is turned on (at instant t_2). This makes the capacitor start discharge through the devices, D_1, resonant inductor L_{r1}, auxiliary switch S_{1A} and resonant inductor L_{r1} as shown in Fig. 4(b).

Mode 3 [$t_2 – t_3$]

At the end of the discharge at instant t_3, the polarity of the voltage across the capacitor C_r reverses. While D_1 is still carrying current, the gate signal of the main device S_1 is made high (instant t_2) and the device goes to ON state. The load current in the main switch starts flowing when the voltage drop across it is zero. Resonance phenomenon completes at instant t_3 with capacitor, C_r attaining the voltage polarity as shown in Fig. 4(c).

Mode 4 [$t_3 – t_4$]

The resonant capacitor voltage polarity will be in the same state as shown in during this period. Since S_1 is ON, the current flows from dc bus to FES machine as shown in Fig. 4(c).

Mode 5 [$t_4 – t_5$]

The auxiliary switch S_{2A} is turned ON at instant t_4. The capacitor voltage changes its polarity as the charging current flows from dc+ through S_1, L_{r2}, L_{r1}, S_{2A} and back to dc- as shown in Fig. 4(d). This makes the capacitor voltage polarity appropriate to make it ready for turning OFF the main switch S_1 as shown in Fig. 4(e).

Mode 6 [$t_5 – t_6$]

The resonant capacitor voltage polarity will continue to be in the same state as shown in during this period. Since S_1 is ON, the current flows from dc bus to FES machine as shown in Fig. 4(e).

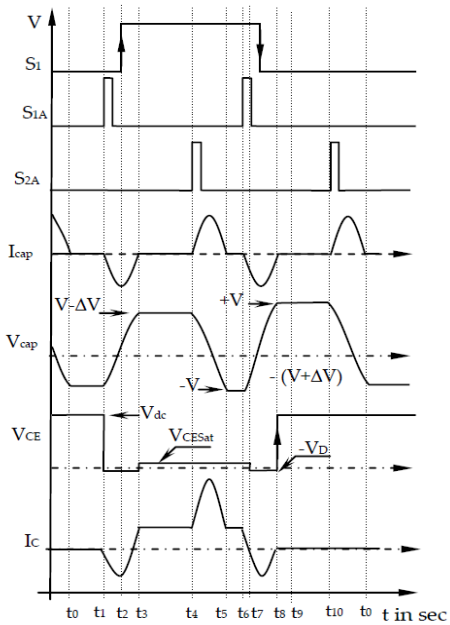


Fig. 3. Control pulses, current/voltage waveforms(buck)

Mode 7 [$t_6 – t_7$]

Just before the switch S_1 is required to be turned off, the auxiliary switch S_{1A} is turned on again. This makes the current through the main switch S_1 to reduce as the load current is shared by the capacitor C_r. Once the capacitor current becomes equal to the load current, the current through the main switch becomes zero as shown in Fig. 3 at t_7.

Mode 8 [$t_7 – t_8$]

Capacitor discharges its remaining charge through D_1 as shown in Fig. 4(g). At the end of the discharge at instant t_8, the polarity of the voltage across the capacitor C_r reverses. During the interval t_7 to t_8 the gate signal to the main device S_1 is removed, when the current through this is already zero. The current through D1 becomes zero at t_8.

Mode 9 [$t_8 – t_9$]

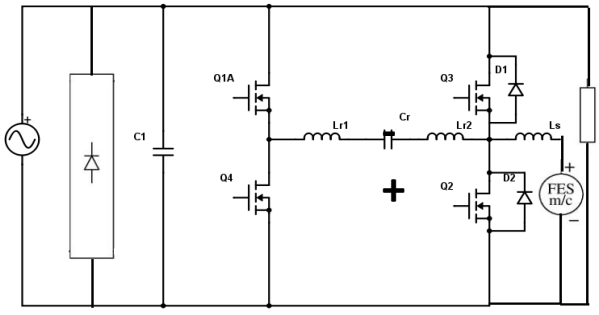
At the beginning of this mode, the capacitor has a voltage with a polarity as shown in Fig. 4(h). This is not the desired polarity of C_r and is required to be reversed for the next turn ON operation of S_1.

Mode 10[$t_9 – t_{10}$]

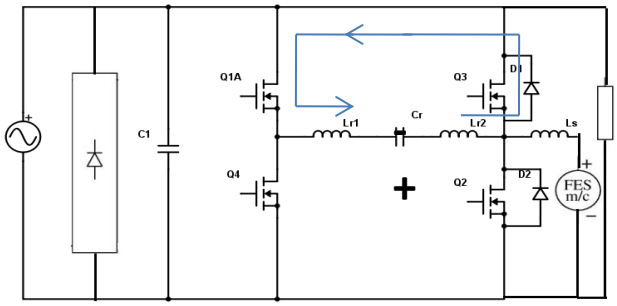
No change in the status of circuit in this mode. The capacitor voltage continues with the polarity as shown in Fig. 4(h).

Mode 11 [$t_{10} – t_0$]

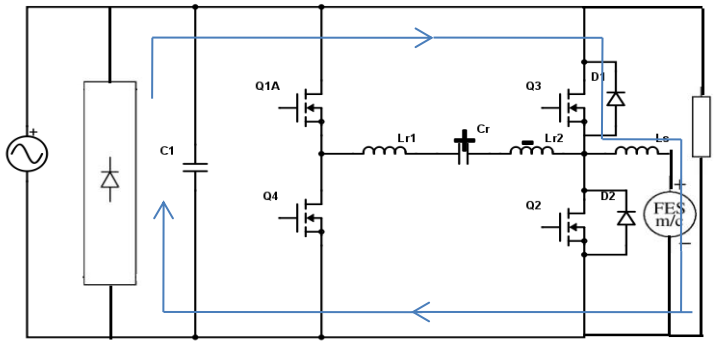
The auxiliary switch S_{2A} is tuned ON at instant t_{10}. The resonant capacitor voltage changes its polarity as the discharge current flows from C_r+ through L_{r1}, S_{2A}, D_2, L_{r2} and back to C_r- as shown in Fig. 4(i). At the instant, t_0 the capacitor acquires voltage with proper polarity required to make it ready for the next cycle as shown in Fig. 4(a).



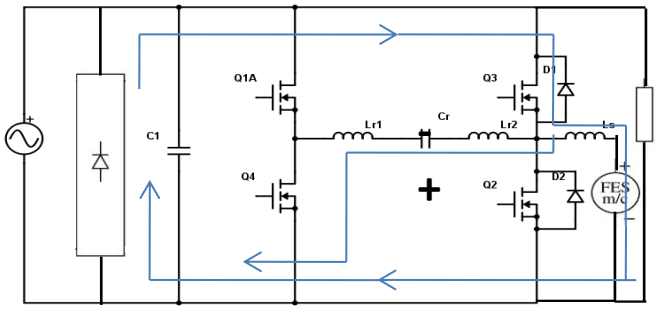
(a) Time interval: t_0-t_1



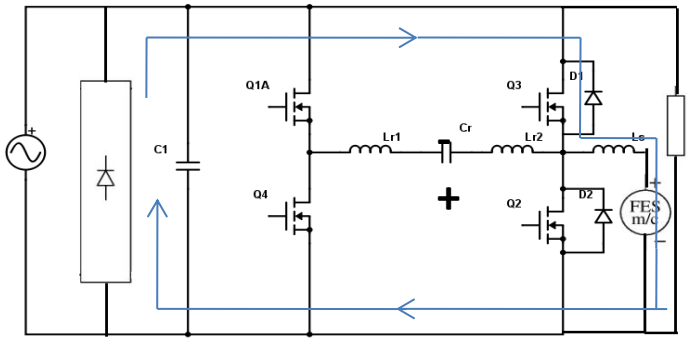
(b) Time interval: t_1-t_2



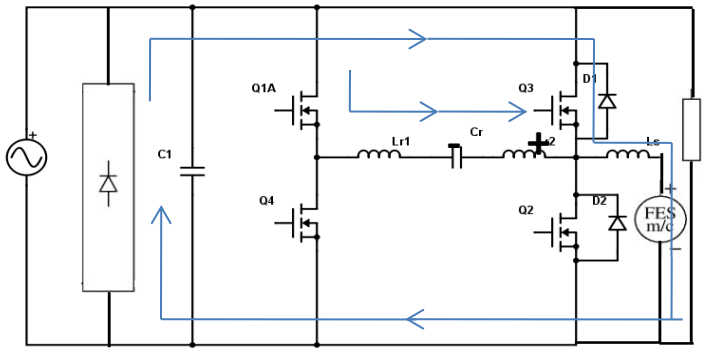
(c) Time interval: t_2-t_3



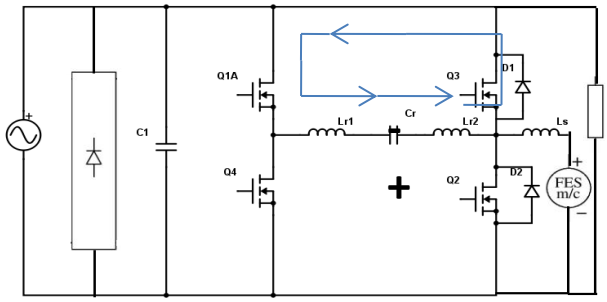
(d) Time interval: t_3-t_4



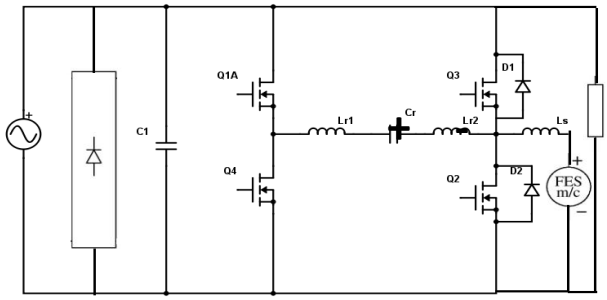
(e) Time interval: t_4-t_5



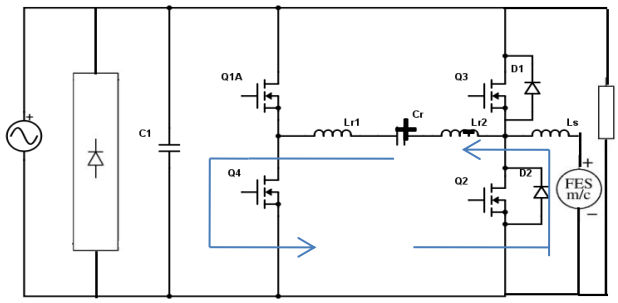
(f) Time interval: t_6-t_7



(g) Time interval t_7-t_8



(h) Time interval: t_8-t_9



(i) Time interval: t_9-t_{10}

Fig. 4. Current path in the circuit and device status in buck mode of operation

3.2. Switching waveforms and analysis in boost mode

In this mode, the power flow from the FES system to the dc bus. The switch S_2 is gated with high frequency pulses whose width is adjusted to get the required boosted dc bus voltage. Control pulses and anticipated waveforms across the power components are shown in Fig. 5.

By referring to Fig. 5 and Fig. 6, the analysis of the circuit is carried out as follows:

Mode 1[t_0 – t_1]

The capacitor C_r is charged with the voltage polarity shown in Fig. 6(a).

No change in status.

Mode 2 [t_1 – t_2]

Just before the switch S_2 is turned on, the auxiliary device S_{2A} is turned on at instant t_1 and the capacitor discharges through the devices L_{r1}, S_{2A}, L_{r2} and D_2 as shown in Fig. 6(b).

Mode 3 [t_2 – t_3]

At instant t_2, gate pulse of the main device S_2 is made high, while freewheeling diode is still carrying the current. Current through the main device S_2 increases, shorting the source through the inductor L_s to ground. The capacitor Cr supplies part of this current as shown in Fig. 6(c) .At the end of discharge (at instant t_3), the capacitor current becomes zero and its voltage polarity reverses as shown in Fig. 6(d) with the magnitude equal to (V -V). Main device S_2 continues to conduct.

Mode 4 [t_3 – t_4]

During this period the resonant capacitor voltage polarity will continue to be in same state as shown in Fig. 6(d). Since S_2 is ON, the current flows from positive of FES machine to series inductor L_s, S_2 and back to negative of FES machine as shown in Fig. 6(d). Some part of the energy of FES machine is transferred to inductor L_s.

Mode 5 [$t_4 – t_5$]
Load current continues to flow through the main switch S_2. The auxiliary switch S_{1A} is tuned ON at instant t_4. The capacitor voltage changes its polarity as the charging current flows from + dc bus through S_{1A}, L_{r1}, L_{r2}, S_2 and back to - dc bus as shown in Fig. 6(e). This makes the capacitor change its polarity and makes it ready for turning OFF the main switch S_2 as shown in Fig. 6(f).

Mode 6 [$t_5 – t_6$]
No change in the device state takes place in this period. The generator current continues to flow through the main switch S_2.

Mode 7 [$t_6 – t_7$]
Just before the switch S_2 is required to be turned OFF, the auxiliary device S_{2A} is turned on again. This result in reduction of current through S_2 as the inductor current L_s is shared by the capacitor C_r as shown in Fig. 6(g) .Once the capacitor current reaches the value of inductor current, the current through the switch S_2 becomes zero at t_7 as shown in Fig. 5.

Mode 8 [$t_7 – t_8$]
Capacitor Cr will be discharging its remaining charge through D_2 as shown in Fig. 6(h). At the end of the discharge (at instant t_8) the polarity of the voltage across the capacitor C_r reverses . The gate signal to the main switch S_2 is removed, during the interval t_7 to t_8. When the current through the switch is already made zero.

Mode 9 [$t_8 – t_9$]
Capacitor C_r will have the polarity as shown in Fig. 6(i).

Mode 10 [$t_9 – t_{10}$]
Capacitor C_r will have the polarity as shown in Fig. 6(i).

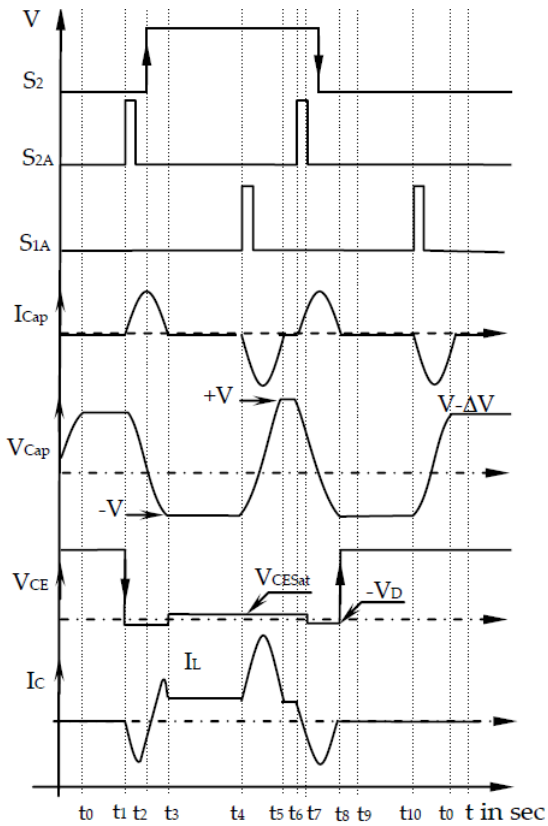
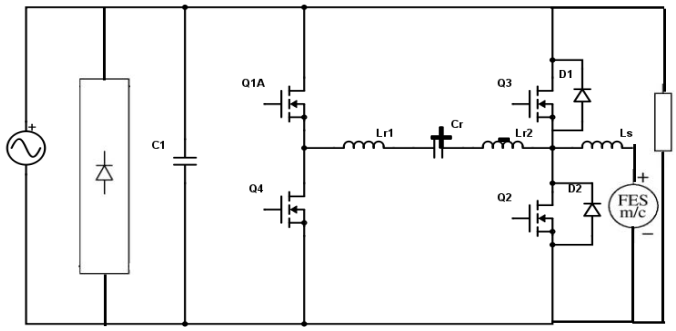
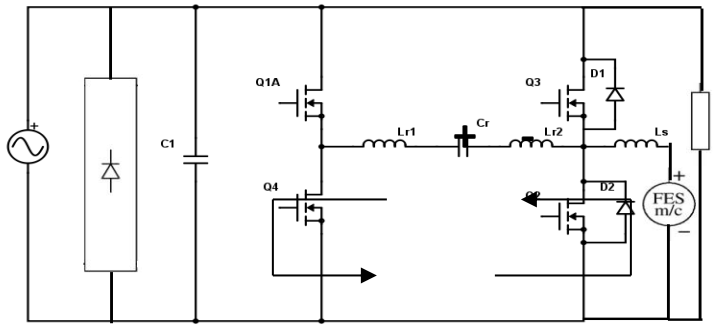


Fig. 5. Control pulses, current/voltage waveforms in boost mode

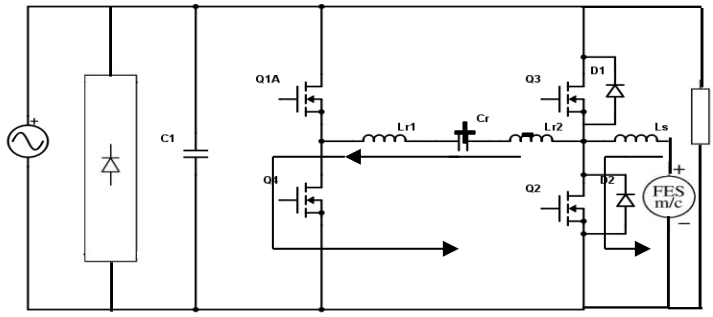
Mode 11 [$t_{10} – t_0$]
The auxiliary switch S_{1A} is tuned ON at instant t_{10}. The resonant capacitor voltage changes its polarity when the discharge current flows through D_1 and S_{1A} as shown in the Fig. 6(j). At this instant the capacitor will acquire the voltage with proper polarity required to make it ready for the next cycle as shown in Fig. 6(a).



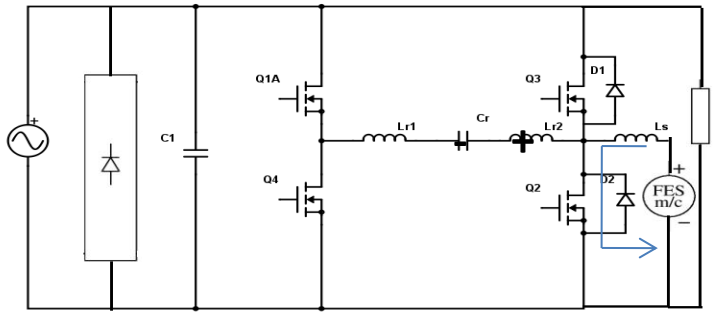
(a) time interval: t_0-t_1



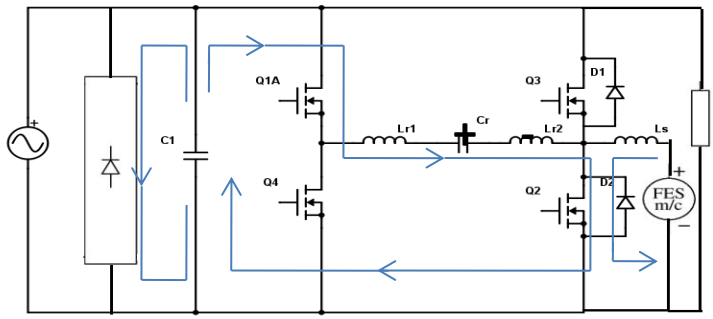
(b) Time interval: t_1-t_2



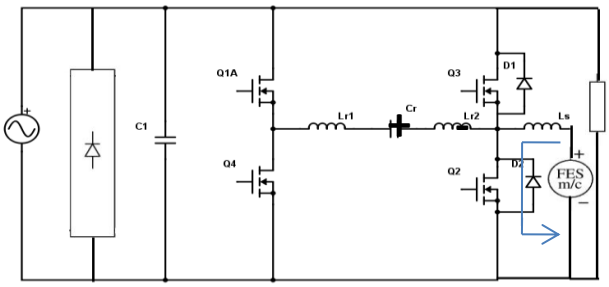
(c) Time interval: t_2-t_3



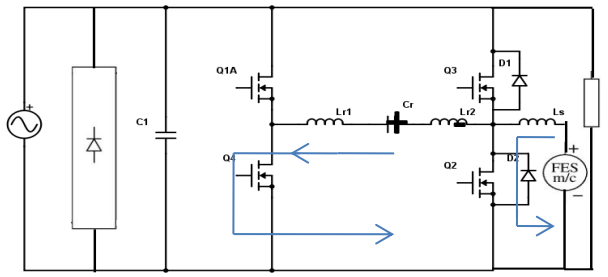
(d) Time interval: t_3-t_4



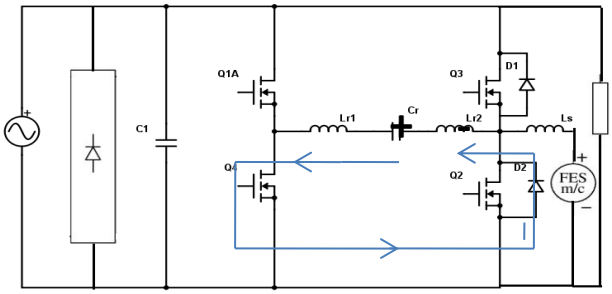
(e) Time interval: t_4-t_5



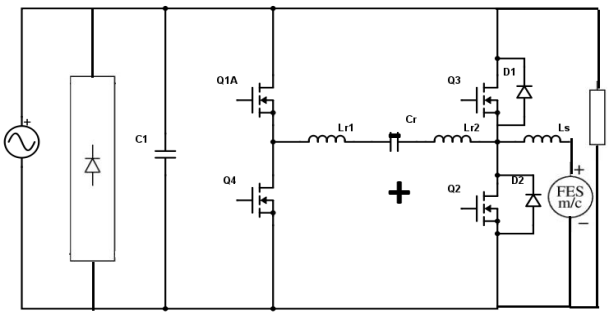
(f) Time interval: t_5-t_6



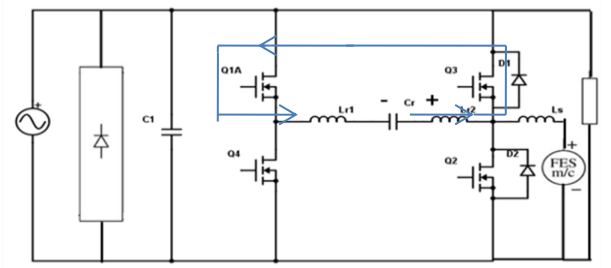
(g) Time interval: t_6-t_7



(h) Time interval: t_7-t_8



(i) Time interval: t_8-t_9



(j) time interval: t_9-t_{10}

Fig. 6. Current path in the circuit and device status in boost mode.

4. Simulation and Experimental Results

The simulation of the proposed topology using the values of components computed in section III was carried out using MATLAB/Simulink software and the results are recorded.

4.1. Simulation results for buck mode of operation

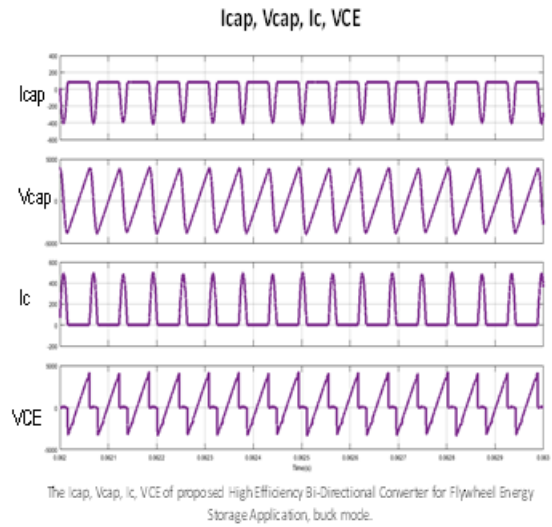


Fig. 8. Simulation results for buck mode of operation of the BDC

4.2. Simulation result for boost mode

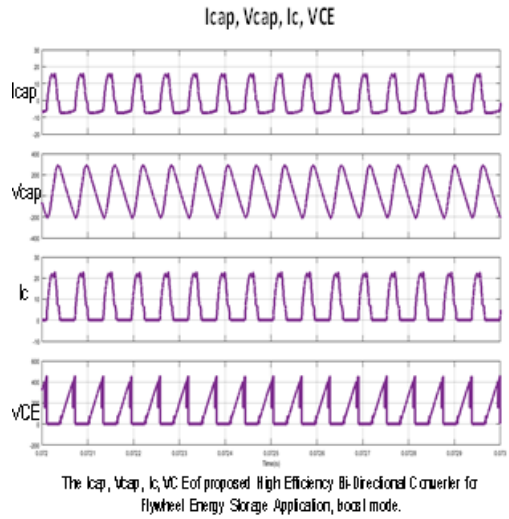


Fig. 9. Simulation results for boost mode operation of the BDC

Likewise, same figures establish that the current through the switching device becomes zero before the voltage across the device starts increasing during OFF transition of the device. It is very clear from the simulation results given in Figs. 8 and 9 for buck and boost mode of operation respectively that the proposed topology will give definite advantage over the previous schemes.

4.3. Experimental results

A lab prototype of the bi-directional converter with ZCT switching technique was built using MOSFET as the main switching device and alsoas the auxiliary device. MOSFET, which is easily available and best suited for high frequency application, was used. Maximum frequency of operation for this device for PWM applications is around 20 kHz. The converter is designed and tested for a reasonable maximum switching frequency of 15.4 kHz. The control logic was implemented and tested at various power levels.

5.Conclusions

This paper has proposed a new topology and control scheme suitable for a BDC application for accomplish ZSPL during turn on as well as turn off transitions of the switching devices. A design methodology has been proposed and simulations of the circuit have been carried out. The experimental testing was done using a bi-directional converter which was built using the proposed topology with a power level of 4.3kW at 340V input. The results were compared with those of hard switched topologies. It is observed that by using the proposed topology there is a saving of power to the extent of 2.5% to 3.5%. Interestingly, the saving power is found to be higher in boost mode as compared to that in buck mode. This is due to the fact that the

device currents will be higher in boost mode as compared to buck mode for the same output power leading to higher losses. This is a advantageous feature for an FES application because the esteemed energy stored in the flywheel can be harvested in the boost mode operation of BDC. Consistency and EMC of the system are improved in this topology at the cost of slight increase in the weight and volume as compared to the hard switching topologies. It is observed that Quasi Resonant Transition (QRT) or Resonant Transition (RT) switching technique can make the turn off losses zero when MOSFET is used as the switching device. Therefore, the proposed topology is good for applications where MOSFET is used as envisaged earlier. Proposed design has been verified and validated with the experimental results.

A limitation of the proposed scheme is that the optimum values of the resonant components depend on operating load conditions which is a drawback of the proposed topology. Space requirement is more. And the energy obtained is kinetic energy which cannot be stored for long time. Also, this topology is not suitable for applications with high operating frequencies

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